What is claimed is:

1. A gateway for interconnecting wireless and wireline networks, comprising:

a plurality of micro-engines, each of said micro-engines comprising a memory for storing instructions for performing data flow processing of data packets for a respective stage of a pipeline process for interconnecting said wireless and said wireline networks; and

a main processor for performing control processing of data packets for said pipeline process;

wherein only said main processor comprises an operating system.

2. The gateway of claim 1, further comprising a memory that is shared by the micro-engines and the main processor.

3. The gateway of claim 2, wherein said shared memory comprises a multi-level hierarchy.

4. The gateway of claim 3, wherein said shared memory comprises at least one SDRAM memory bank and at least one SRAM memory bank.

5. The gateway of claim 4, wherein said SRAM memory bank stores at least one of active sessions, data structures and tables.

6. The gateway of claim 4, wherein a Packet Routing Table is stored in said SRAM memory bank.

7. The gateway of claim 4, wherein said SDRAM memory bank stores at least one of packet payload and inactive always-on session overflow from said SRAM memory bank.

8. The gateway of claim 1, wherein the data flow processing of data packets for each stage of the pipeline process is performed by at least one micro-engine.

9. The gateway of claim 1, wherein each micro-engine performs the data flow processing of data packets for at least one stage of the pipeline process.

10. A method of interconnecting wireless and wireline networks, comprising:

performing data flow processing of data packets for respective stages of a pipeline process for interconnecting said wireless and said wireline networks via respective micro-engines, each of said micro-engines comprising a memory for storing instructions for performing the respective data flow processing; and

performing control processing of data packets for said pipeline process using a global main processor.

11. The method of claim 10, wherein each of the micro-engines associated with a respective stage of the pipeline process performs a table look-up function using a respective data packet header to determine if a data packet is capable of being processed by the respective micro-engines.

12. The method of claim 11, wherein if a table look-up fails, the respective data packet is forwarded to said main processor for control processing.

13. The method of claim 12, wherein said main processor configures data structures of received data packets for further data flow processing by respective micro-engines of subsequent stages of the pipeline process.

14. The method of claim 11, wherein if a table look-up is successful, the data flow processing of a data packet is performed by at least one respective micro-engine.

15. The method of claim 10, wherein after said global main processor performs the control processing of a received data packet, the processed data

packet is forwarded to a queue for further data flow processing by said micro-engines.

16. The method of claim 10, wherein the data flow processing of data packets in various stages of said pipeline process is performed in parallel by respective micro-engines.

17. The method of claim 10, wherein the data flow processing of data packets in each of the stages of the pipeline process is performed by at least one respective micro-engine.

18. The method of claim 10, wherein each of the micro-engines performs the data flow processing of data packets for at least one stage of the pipeline process.

19. The method of claim 10, wherein the data flow processing of a data packet for each of the stages of the pipeline process is performed in the sequential order of the pipeline process by respective micro-engines.

20. An apparatus for interconnecting communication networks, comprising:

a plurality of micro-engines, each of said micro-engines comprising a memory for storing instructions for performing data flow processing of data packets for a respective stage of a pipeline process for interconnecting said communication networks; and

a main processor for performing control processing of data packets for said pipeline process;

wherein only said main processor comprises an operating system.